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10/825,033	04/14/2004	Yoshikazu Fujimori	12844.15USD1	7384

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EXAMINER	
OWENS, BETH E	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,033	FUJIMORI, YOSHIKAZU	
	Examiner	Art Unit	
	Beth E. Owens	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/218,988.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04142004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it contains grammatical errors and does not clearly describe the invention. Correction is required. See MPEP § 608.01(b).

2. Please replace the amended first line of the Specification with: --This application is a divisional of parent application serial number 10/218,988, filed 13 August 2002, now U.S. Patent No. 6,740,532, issued 25 May 2004.--

3. Please replace the current Specification with the substitute Specification for the parent application filed 26 January 2004.

Claim Objections

4. The following Claims are objected to because of the following informalities:

Claim 2, line 1: please delete "substance".

Claim 2, line 3: please insert --a-- before "solution".

Claim 2, line 3; please replace "an" with --the--.

Claim 2, line 3: please delete "substance".

Claim 3, lines 1 and 2: please delete "substance".

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 and 6-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claims are written in poor grammatical form and are confusing; also the use of "substance" after "ferroelectric" in reference to the thin film is redundant and needs to be deleted, as was done in the parent application 10/218,988. Rewriting the claims in the following forms would overcome these rejections.

Claim 1: A method of forming a ferroelectric thin film, comprising:

forming a seed layer containing an ultra-fine particle powder comprised of an element constituting the ferroelectric thin film to be subsequently formed on a surface of the substrate; and

forming the ferroelectric thin film on the seed layer.

Claim 6: A method of forming a ferroelectric memory including an FET of an MFMIS structure, said method comprising:

forming a gate insulating film on a semiconductor substrate and between source-drain regions;

forming a floating gate on the gate insulating film;

forming a ferroelectric layer on the floating gate; and

forming a control gate on the ferroelectric layer,

wherein forming the ferroelectric layer comprises:

forming a seed layer on a surface of the floating gate, the seed layer containing an ultra-fine particle powder comprised of an element constituting a ferroelectric thin film to be subsequently formed on the seed layer; and

forming the ferroelectric thin film on the seed layer.

Claim 7: A method of forming a ferroelectric memory including an FET of an MFMIS structure, said method comprising:

forming a gate insulating film on a surface of a semiconductor substrate and between source-drain regions;

forming a floating gate on the gate insulating film;

forming a ferroelectric layer on the floating gate; and

forming a control gate on the ferroelectric layer,

wherein forming the ferroelectric layer comprises:

applying a liquid, subsequently to be formed into a ferroelectric thin film, on a surface of the floating gate, the liquid containing an ultra-fine particle powder comprised of an element constituting the ferroelectric thin film; and

baking the liquid applied to the surface of the floating gate, thereby forming the ferroelectric thin film.

Claim 8: A method of forming a ferroelectric memory comprising:

forming an FET including a gate electrode formed on a surface of a semiconductor substrate between source-drain regions, the source-drain regions formed on the surface of the semiconductor substrate through a gate insulating film; and

forming a ferroelectric capacitor connected with one of the source-drain regions of the FET through a storage node contact,

wherein forming the ferroelectric capacitor comprises:

forming a first electrode;

applying a liquid, subsequently to be formed into a ferroelectric thin film, on a surface of the first electrode, the liquid containing an ultra-fine particle powder comprised of at least one element constituting the ferroelectric thin film; and

forming the ferroelectric thin film by baking the liquid applied to the surface of the first electrode; and

forming a second electrode on the ferroelectric thin film.

Claim 9: A method of forming a ferroelectric memory comprising:

forming an FET including a gate electrode formed on a surface of a semiconductor substrate between source-drain regions, the source-drain regions formed on the surface of the semiconductor substrate through a gate insulating film; and

forming a ferroelectric capacitor connected with one of the source-drain regions of the FET through a storage node contact,

wherein forming the ferroelectric capacitor comprises:

forming a first electrode;

forming a seed layer on a surface of the first electrode, the seed layer containing an ultra-fine particle powder comprised of an element constituting a ferroelectric thin film to be subsequently formed on the seed layer; and

forming the ferroelectric thin film on the seed layer.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie et al.

In regards to Claims 7 and 8:

Horie et al. teach a method for forming ferroelectric thin films for general use and specific use in MFIS-FET and MFMIS-FET memory structures:

column 1, lines 13-25: Thin films of metal oxides are generally used as oxide dielectric and insulating films of SiO_2 and Ta2O.sub.5, high dielectric and ferroelectric films having a Perovskite structure represented by ABO_3, in particular, of $BaTiO_3$, $Ba(Ti,Hf,Zr)O_3$, $SrTiO_3$, $(Ba,Sr)TiO_3$, $(Ba,Sr,Ca)TiO_3$, $PbTiO_3$, $PbZrO_3$, $Pb(Nb,Ti)O_3$, $Pb(Zr,Ti)O_3$, PLZT, $YMnO_3$, and $(La,Sr)MnO_3$, ferroelectric films having other structures, of $SrBi_2Ta_2O$, $SrBi_2(Ta,Nb)_2O_9$, $Sr_2(Ta,Nb)O_7$, $(Sr,Ba)Nb_2O_6$, $SrTa_2O_6$, $Bi_4Ti_3O_{12}$, and Bi_2SiO_5, electrode films of RuO_2, RuO_4, $SrRuO_3$, and IrO_2, and buffer films of Y_2O_3, CeO_2, ZrO_2, and $(Ce,Zr)O_2$ for memory materials of MFIS-FET, MFMIS-FET structures and films exemplified by ferroelectric films.

column 2, lines 53-61: The metal or metal compound particles may be heated or annealed in an oxidizing gas atmosphere to produce a thin film of metal oxide. The thin film of metal oxide may be made of SiO_2, Ta_2O_5, $BaTiO_3$, $Ba(Ti,Hf,Zr)O_3$, $SrTiO_3$, $(Ba,Sr)TiO_3$, $(Ba,Sr,Ca)TiO_3$, $PbTiO_3$, $PbZrO_3$, $Pb(Nb,Ti)O_3$, $Pb(Zr,Ti)O_3$, PLZT, $YMnO_3$, $(La,Sr)MnO_3$, $SrBi_2Ta_2O_9$, $SrBi_2(Ta,Nb)_2O_9$, $Sr_2(Ta,Nb)O_7$, $(Sr,Ba)Nb_2O_6$, $SrTa_2O_6$, $Bi_4Ti_3O_{12}$, Bi_2SiO_5, RuO_2, RuO_4, $SrRuO_3$, IrO_2, MFIS-FET,Y_2O_3, CeO_2, ZrO_2, or $(Ce,Zr)O_2$.

column 3, lines 43-45: First, an ultrafine particle dispersion liquid is prepared by dispersing ultrafine particles at least partly made of metal into a given organic solvent.

column 3, lines 60-63: The metal M may be Si, Ta, Ca, Sr, Ba, Ti, Bit Pb, Nb, Y, Mn, Al, Hf, Zr, Ce, Ir, Ru, En, Mg, La, Ga, Tm, Cu, Tb, Eu, Sm, or WI which may be selected depending on how the thin film will be used.

column 4, lines 54-67: Then, the ultrafine particle dispersion liquid is applied to the surface of a substrate. For example, the substrate is uniformly coated with the ultrafine particle dispersion liquid by a spin coating process. The substrate may be coated with the ultrafine particle dispersion liquid to a uniform thickness by adjusting the spinning speed, and properties of the ultrafine particle dispersion liquid which include the viscosity, the surface

tension, etc. If the ultrafine particle dispersion liquid is applied to a local area or small spot on a substrate, then the substrate may be coated with the ultrafine particle dispersion liquid by an ink jet process. If the thickness uniformity or coating efficiency is not of prime importance, then the substrate may be coated using a brush with the ultrafine particle dispersion liquid.

column 5, lines 39-60: The ultrafine particles left on the substrate by drying the ultrafine particle dispersion liquid are heated to at least a temperature at which the organic materials is released from the metal core or at least a temperature at which the organic materials is decomposed, so that the organic material is released from the metal cores or dissolved away and at the same time the metal or metal compound particles are melted and joined together in a predetermined atmosphere. In this manner, a thin film of metal or metal compound is formed on the surface of the substrate and bonded thereto with a sufficient bonding strength between the substrate and the thin film. If a thin film of metal oxide is to be produced, then the ultrafine particles are heated in an oxidizing gas atmosphere. If a thin film of metal sulfide is to be produced, then the ultrafine particles are heated in a hydrogen sulfide atmosphere. If a thin film of metal nitride is to be produced, then the ultrafine particles are heated in a nitriding gas atmosphere such as of nitrogen or ammonia. The ultrafine particles may be heated by radiation heating such

as resistance heating, infrared heating, far-infrared heating, or the like, or by microwave heating, laser beam heating, plasma heating, or the like.

column 6, lines 6-16: The melted and joined metal particles are annealed into a crystalline state. If the ultrafine particles were only heated as described above, they might be remain in an amorphous state. Therefore, if a thin film of metal oxide is to be produced, then the melted and joined metal particles are annealed in an oxidizing gas atmosphere. If a thin film of metal sulfide is to be produced, then the melted and joined metal particles are annealed in a hydrogen sulfide atmosphere. If a thin film of metal nitride is to be produced, then the melted and joined metal particles are annealed in a nitriding gas atmosphere. In this manner, the metal is crystallized.

Horie et al. however, are silent in regards to the method of forming the ferroelectric memory structures of claims 7 and 8 which include ferroelectric thin films formed by Horie et al.'s method. Examiner takes Official Notice that the general method of fabricating an FET of an MFMIS structure in claim 7 and the formation of the ferroelectric memory of claim 8 containing a ferroelectric capacitor would have been well known to one ordinarily skilled in the art at the time the invention was made. Therefore, for the purpose of producing more sufficient bonding strength between the substrate and the ferroelectric thin film than that produced by a sol-gel process, and for

producing the thin film inexpensively and more quickly without the need for a large-scale evacuating apparatus necessary for a CVD process, it would have been obvious to have combined Horie et al.'s ferroelectric thin film manufacturing method with that of known methods for forming ferroelectric memory structures.

Allowable Subject Matter

9. The following is a statement of reasons for the indication of allowable subject matter:

There is no available prior art nor obvious motivation to combine elements of prior art which teaches a method for forming a ferroelectric thin film, comprising: forming a seed layer containing an ultra-fine particle powder comprised of an element constituting the ferroelectric thin film to be subsequently formed on a surface of the substrate; and forming the ferroelectric thin film on the seed layer;

and:

A method of forming a ferroelectric memory including an FET of an MFMIS structure, said method comprising: forming a gate insulating film on a semiconductor substrate and between source-drain regions; forming a floating gate on the gate insulating film; forming a ferroelectric layer on the floating gate; and forming a control gate on the ferroelectric layer, wherein forming the

ferroelectric layer comprises: forming a seed layer on a surface of the floating gate, the seed layer containing an ultra-fine particle powder comprised of an element constituting a ferroelectric thin film to be subsequently formed on the seed layer; and forming the ferroelectric thin film on the seed layer;

and:

A method of forming a ferroelectric memory comprising: forming an FET including a gate electrode formed on a surface of a semiconductor substrate between source-drain regions, the source-drain regions formed on the surface of the semiconductor substrate through a gate insulating film; and forming a ferroelectric capacitor connected with one of the source-drain regions of the FET through a storage node contact, wherein forming the ferroelectric capacitor comprises: forming a first electrode; forming a seed layer on a surface of the first electrode, the seed layer containing an ultra-fine particle powder comprised of an element constituting a ferroelectric thin film to be subsequently formed on the seed layer; and forming the ferroelectric thin film on the seed layer.

10. Claims 1-3, 6 and 9 would be allowable if rewritten or amended to overcome all objections and the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims, if applicable.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Beth E. Owens, Ph.D., whose telephone number is 571.272.1882 and fax number for unofficial communications is 571.273.1882.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms, can be reached on 571.272.1869. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306 for official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571.272.2800.

BEO

BEO 09.07.04

VAN THU NGUYEN
PRIMARY EXAMINER